Quasi-Linear Amplification Using Self Phase Distortion Compensation Technique

Hitoshi Hayashi, *Member, IEEE,* Masashi Nakatsugawa, *Member, IEEE,* and Masahiro Muraguchi, *Member, IEEE*

***Abstract*—This paper demonstrates a self phase distortion compensation technique to realize linear power amplifiers, in which the positive phase deviation from a common-source FET and the negative phase deviation from a common-gate FET cancel each other. It is confirmed both theoretically and experimentally that increasing the drain-to-source conductance, G_d, causes the self phase distortion compensation effect. An experimental power amplifier for L-band personal communications systems, which employs the cascode connection, shows good phase deviation performance. More than 20-dB gain, 21-dBm output power, and 50% power added efficiency are obtained along with the adjacent channel interference of −52 dBc in 192-kHz bands at 600-kHz offset frquency from 1.9 GHz at the operating voltage of only 3 V. The demonstrated performances satisfy the specifications for the 1.9-GHz Japanese Personal Handy-phone System (PHS) utilizing the $\pi/4$-shift QPSK modulation scheme. The proposed technique is suitable for MMIC design, and allows the design of handsets that are small, lightweight, and have long operating times.**

I. Introduction

IT IS IMPORTANT in mobile and personal communication systems [1] to extend the operation time, and to minimize the volume and weight of handy phone sets. One of the most effective ways of reducing volume and weight is to reduce the battery size, because the battery is the largest and heaviest device used in handy phone sets. However, when the battery size is decreased, its capacity is decreased proportionally. Therefore, the power consumption of handy phone circuits should be drastically reduced.

Since the power amplifiers (PA) consume a large portion of the total dc power in the handsets for the Japanese Personal Handy-phone System (PHS), highly efficient PA's that operate near the saturation region are required.

In order to use the radio spectrum more efficiently, PHS adopts the narrow-band $\pi/4$-shift QPSK modulation scheme which does not have a constant envelope. The nonlinearity of conventional high-efficiency amplifiers (class C or F) increases adjacent channel interference when they process $\pi/4$-shift QPSK signals. Many investigations into distortion compensation considered the phase distortion effect to be negligible [2].

Phase distortion, however, significantly increases with AM-PM conversion near the saturation region, resulting in increased adjacent channel interference. It is crucial to realize low adjacent channel interference and high efficiency simultaneously with operation near the saturation region while suppressing the phase nonlinearity.

Studies on some large signal GaAs MESFET models [3], [4] and analysis of large signal GaAs MESFET amplifier characteristics [5] have been reported. Recently, Ikeda showed details of the phase distortion mechanism of a GaAs MESFET power amplifier [6]. He pointed out that the phase deviation of the common-source FET (CSF) increases with the input power and that phase variation could be reduced by combining the phase deviation effect of the drain-to-gate conductance, G_{dg}, with that of the drain-to-source conductance, G_d, at saturation region. However, no method of utilizing this effect was given, only its effect on output impedance was mentioned.

There were also some reports on achieving amplitude control while minimizing the phase variation by using the dual-gate FET's [7]. The dependence of gain, phase, and stability on the dual-gate FET's second gate termination has also been considered [8]. None of these papers, however, has the goal of improving AM-PM conversion at the saturation region.

This paper describes an effective way of increasing PA efficiency by improving linearity while satisfying the PHS specifications.

II. Phase Distortion Compensation Method

A. Input-Output Phase Characteristics of CSF and CGF

Due to the fact that the CSF delivers the output power out of phase while the common-gate FET (CGF) does so in phase, their AM-PM conversion at near saturation region are also expected to have opposite behaviors. Accordingly, we measured the large-signal phase distortion characteristics of the CSF and CGF.

A CSF and a CGF were fabricated and tested. Measured phase deviation versus the output power is shown in Fig. 1. The input power level was varied from −20–14 dBm. The phase deviation means the phase deviation from the linear region. The saturation current (I_{dss}), W_g and L_g of FET's were 416 mA, 1,920 μm, and 0.7 μm, respectively. FET performance was measured at a drain voltage of 3 V and an idle drain current of $I_{dss}/5$. Phase deviations were measured using the HP 8753C network analyzer's power sweep function. Both FET's were fabricated at the same time by using a type of selected ion implantation process. Their input and output impedances were small-signal-gain matched with slide-screw tuners. The operating frequency was 1.9 GHz. As the input power increases, the phase deviation of the CSF increases while that of the CGF decreases.

Manuscript received August 22, 1994; revised August 1, 1995.

The authors are with the NTT Wireless Systems Laboratories, 1-2356 Take, Yokosuka-shi, Kanagawa 238-03, Japan.

IEEE Log Number 9414853.

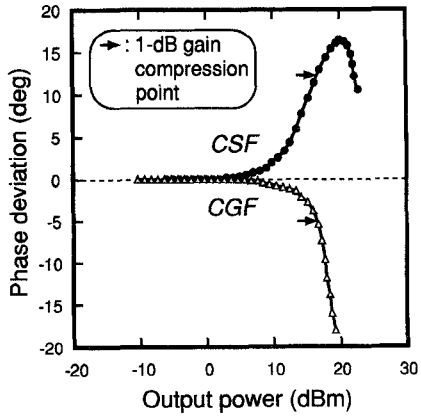


Fig. 1. Phase deviation versus the output power of the CSF and CGF.

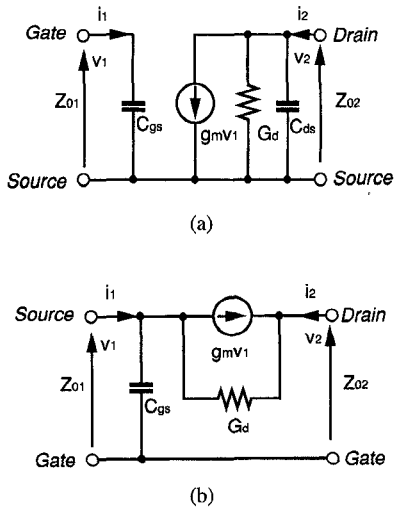


Fig. 2. Simplified equivalent circuit analysis of the different phase deviation between CSF and CGF. (a) CSF. (b) CGF.

B. Analysis and Experiments of FET Model

FET phase distortion has four independent origins [6]: Gate-to-source capacitance, C_{gs}; gate-to-source conductance, G_{gs}; drain-to-source conductance, G_d; and drain-to-gate conductance, G_{dg}. In the near-saturation region, the phase deviation can be attributed to an increase in G_d and C_{gs}. Of particular interest is the behavior of the dominant sources of phase distortion effects, i.e., G_d and C_{gs}.

The contribution of G_d and C_{gs} to the phase deviation is discussed here using the simplified equivalent circuits of the CSF and CGF shown in Fig. 2 with reference to Appendixes A and B.

In the case of the CSF, the phase of S_{21} is

$$\text{phase}(S_{21}) = \pi - \tan^{-1} \cdot \left[\frac{\omega\{(C_{gs}Z_{01} + C_{ds}Z_{02}) + G_d C_{gs} Z_{01} Z_{02}\}}{1 + G_d Z_{02} - \omega^2 C_{gs} C_{ds} Z_{01} Z_{02}} \right]. \quad (1)$$

The differentials of G_d and C_{gs} are thus

$$\frac{\partial_{\text{phase}}(S_{21})}{\partial G_d} > 0, \quad \frac{\partial_{\text{phase}}(S_{21})}{\partial C_{gs}} < 0. \quad (2)$$

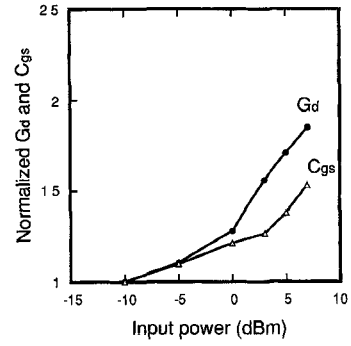


Fig. 3. Variation of the normalized values of the two nonlinear elements (G_d, C_{gs}).

The phase deviation increases with G_d, but decreases with C_{gs}. On the other hand, in the case of the CGF, the phase of S_{21} is

$$\text{phase}(S_{21}) = \tan^{-1} \left[\frac{-\omega C_{gs} Z_{01}(1 + G_d Z_{02})}{1 + (g_m + G_d) Z_{01} + G_d Z_{02}} \right]. \quad (3)$$

Thus the differentials of G_d and C_{gs} are

$$\frac{\partial_{\text{phase}}(S_{21})}{\partial G_d} < 0, \quad \frac{\partial_{\text{phase}}(S_{21})}{\partial C_{gs}} < 0. \quad (4)$$

The phase deviation decreases in proportion to the increases in G_d and C_{gs}. From (2) and (4), it is found that only G_d causes the difference in the phase deviation between the two FET's. In addition, it is clear from (1) and (3) that the phase deviation of the CSF is not directly influenced by g_m, while the phase deviation of the CGF decreases as g_m decreases.

It was confirmed experimentally that G_d is the dominant parameter of the phase deviation. The values of G_d and C_{gs} extracted by fitting S parameters measured at each input power are shown in Fig. 3. For the FET device, an equivalent circuit parameter was generated from S parameter measurements between 1.5–3 GHz. The measured data covering the range from −10–7 dBm were obtained with the FET biased at a drain voltage of 3.0 V and an idle drain current of $I_{dss}/5$. The values of C_{gs} and G_d are normalized by 1.27 pF and 6.25 mS. The variation of normalized G_d is greater than that of C_{gs} at all input power levels. From these results, we conclude that G_d is responsible for the difference in phase deviation between the CSF and CGF in the saturation region.

C. Bias Dependence of Phase Shift Behavior

Fig. 4 shows the measured output power and phase deviation at the 1-dB gain compression point (P_{-1}) versus the V_{gs} of the CSF and CGF. The measured data covers V_{gs} from −0.6 to −1.2 V, which corresponds to an idle drain current from $I_{dss}/2$ to $I_{dss}/5$, at a drain voltage of 3.0 V. The output power of the CSF at P_{-1} slightly decreases as the bias current reduces from $I_{dss}/2$ to $I_{dss}/5$, while the output power of the CGF at P_{-1} varies little as the bias current reduces from $I_{dss}/2$ to $I_{dss}/5$. The phase deviation increases as the CSF gate bias de-

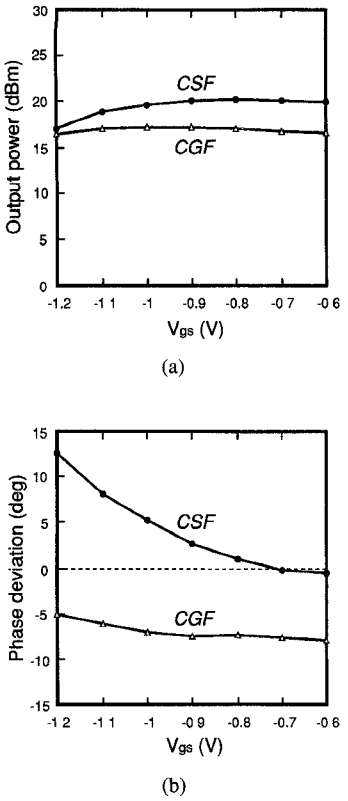


Fig. 4. Output power and phase deviation at P_{-1} versus the V_{gs} of CSF and CGF. (a) Output power. (b) Phase deviation.

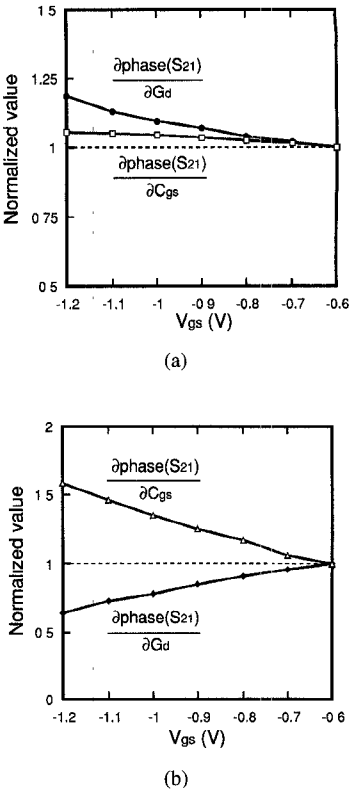


Fig. 5. Variations of the normalized values of the two differentials $(\partial_{\text{phase}}(S_{21})/\partial G_d, \partial_{\text{phase}}(S_{21})/\partial C_{gs})$. (a) CSF. (b) CGF.

creases, while the phase deviation does not change much as the CGF gate bias decreases. We simulated the bias dependence of the differential of the phase of S_{21} using the extracted HP Root FET model [9]. The variations of the normalized values of the two differentials $(\partial_{\text{phase}}(S_{21})/\partial G_d, \partial_{\text{phase}}(S_{21})/\partial C_{gs})$ are shown in Fig. 5. The calculations involved (A-5), (A-6), (B-7), and (B-8). Since the differentials of $\partial_{\text{phase}}(S_{21})/\partial C_{gs}$ in the CSF and $\partial_{\text{phase}}(S_{21})/\partial G_d$ and $\partial_{\text{phase}}(S_{21})/\partial C_{gs}$ in the CGF are negative, the relative amounts are compared in Fig. 5. Normalized values were taken at V_{gs} of -0.6 V and the input power levels of -15 dBm. The input and output impedance values, Z_{01} and Z_{02}, are selected near the output impedances of the FET's, 10 ohms. In the CSF, as an idle drain current varies from $I_{dss}/2$ to $I_{dss}/5$, the differentials of G_d and C_{gs} increase, and the differential of G_d is bigger than the differential of C_{gs} at any bias value. Thus the phase deviation must increase as the gate bias decreases. On the other hand, in the CGF, as an idle drain current varies from $I_{dss}/2$ to $I_{dss}/5$, the differential of G_d falls but the differential of C_{gs} increases. Accordingly, it is expected that the phase deviation varies little as the gate bias decreases.

Given the close dependence of the circuit behavior on device parameter characteristics, the choice of the most suitable FET bias point is an important matter.

D. Input-Output Phase Characteristics of CCF

The idea of compensating the phase distortion by combining a CSF with a CGF, as shown in Fig. 6, is rather obvious. In this case, the CSF acts as a prephase-distortion linearizer of the CGF. It is necessary in this phase distortion circuit to optimize the FET's bias levels.

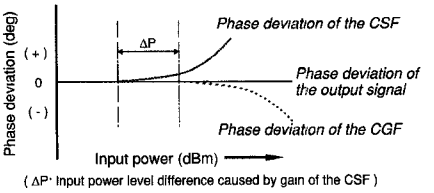


Fig. 6. Principle of phase distortion compensation when combining a CSF with a CGF.

One way of combining a CSF and a CGF is the cascode connection FET (CCF), in which the drain bias circuit and the output matching circuit can be eliminated. In order to cancel out the output phase deviation of the CCF, the saturation level of the CGF should be suitably higher than that of the CSF, as shown in Fig. 6, because the input power level of the CGF is higher due to the gain of the CSF. Fortunately, the combination of the saturation levels of the CSF and CGF can be easily changed by adjusting the gate biases because the allotted supplied drain voltage between the CSF and CGF can be controlled by the gate biases [10].

The contribution of G_d and C_{gs} to the phase deviation is discussed here using the simplified equivalent circuits of the CCF shown in Fig. 7 with reference to Appendix C.

In the case of the CCF, the phase of S_{21} is shown in (5), at the bottom of the next page.

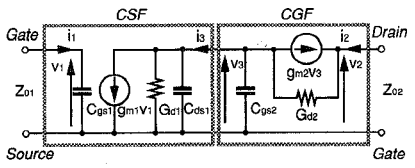


Fig. 7. Simplified equivalent circuit model of the CCF.

Accordingly, the differentials of G_d and C_{gs} are

$$\frac{\partial_{\text{phase}}(S_{21})}{\partial G_{d1}} > 0, \quad \frac{\partial_{\text{phase}}(S_{21})}{\partial C_{gs1}} < 0,$$
$$\frac{\partial_{\text{phase}}(S_{21})}{\partial G_{d2}} < 0, \quad \frac{\partial_{\text{phase}}(S_{21})}{\partial C_{gs2}} < 0. \tag{6}$$

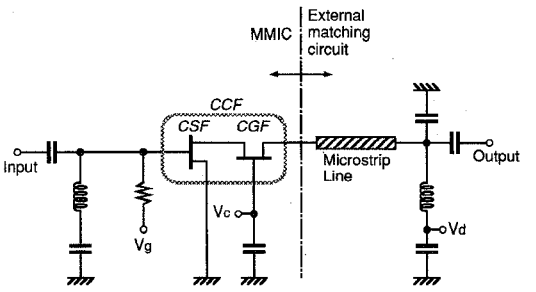
This shows that only G_{d1} always increases phase deviation, while the other differentials always reduce the phase deviation.

We investigated the phase deviation effect caused by the CGF. Comparing the phase equation of the CSF, (1), with the phase equation of the cascode connection, (5), G_{d1} in the CCF is multiplied by the factor of G_{d2}/g_{m2} and C_{ds} in the CSF is replaced by $C_{gs2} * G_{d2}/g_{m2}$. In general, the value G_{d2}/g_{m2} is smaller than 1. Since the phase-increasing effect of G_{d1} in the case of the CCF is smaller than that in the case of the CSF, the phase deviation of the cascode connection generally decreases. To overcome the excessive decrease in phase deviation, it is necessary to enhance the contribution of G_{d1}. The above results indicate that by operating the CSF under low idle current, the phase-increasing effect of G_{d1} is enhanced.

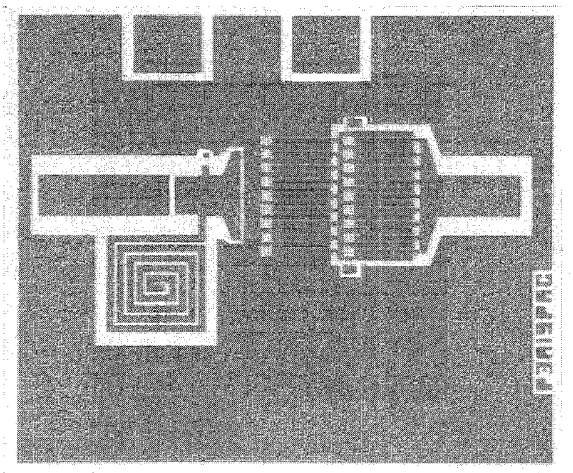
III. Power Amplifier Performance

To experimentally evaluate the ideas presented in the previous sections, a PA was built by combining a CSF and a CGF and putting the output matching circuit outside the FET chip as shown in Fig. 8. The chip size of the MMIC without the output matching circuit was 1.35 mm by 1.13 mm. A microstrip line and chip capacitor on an alumina substrate formed the output matching circuit. This circuit was designed by using load-pull measurement results. The gate width of 2,700 μm was selected by the necessary saturated output power to obtain the adequate output power for the 1.9-GHz Japanese PHS.

Fig. 9 shows the measured output power and phase deviation versus the input power of the CCF power amplifier as a function of the drain bias ratio of the CCF to the CSF, V_{d1}, and the CGF, V_{d2}, at a total drain bias, V_d, of 3 V. Here, the gate bias, V_c, of the CGF is a fixed value of 0 V. The drain



(a)



(b)

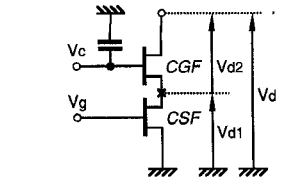
Fig. 8. Configuration of the experimental CCF power amplifier. (a) Circuit configuration. (b) Photograph of MMIC chip.

bias ratio is varied by the gate bias, V_g, of the CSF.

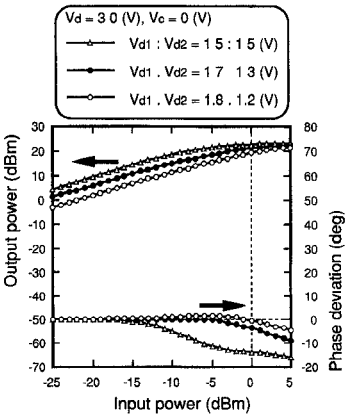
Since the same current must run through both FET's of the CCF, the decrease of the idle drain current of the CSF means the increase of the drain bias ratio of the CSF. As the drain bias ratio of the CSF increases, the phase deviation becomes smaller. A small phase deviation of less than four degrees in spite of the near-saturation region operation of 4-dB gain compression was achieved for output powers up to 21 dBm at the drain bias ratio of $V_{d1} : V_{d2} = 1.7 : 1.3$.

Fig. 10 shows the performance of the amplifier at the drain bias ratio of $V_{d1} : V_{d2} = 1.7 : 1.3$. The power added efficiency (PAE) of 50% was obtained along with the adjacent channel interference of -52 dBc in 192-kHz bands at 600-kHz offset frequency from 1.9 GHz. Here, the 1.9-GHz Japanese PHS employs $\pi/4$-shift QPSK modulation scheme, and the pre-modulation filtering is a root nyquist filter, in which the roll-off factor is 0.5. The bit rate and the channel spacing are set at 384 kb/s and 300 kHz, respectively. The adjacent

$$\text{phase}(S_{21}) = \pi - \tan^{-1}\left[\frac{\omega\left(C_{gs_1}Z_{01} + \frac{C_{gs_2}G_{d_2}}{g_{m_2}}Z_{02} + \frac{C_{gs_1}G_{d_1}G_{d_2}}{g_{m_2}}Z_{01}Z_{02}\right)}{1 + \frac{G_{d_1}G_{d_2}}{g_{m_2}}Z_{02} - \omega^2\frac{C_{gs_1}C_{gs_2}G_{d_2}}{g_{m_2}}Z_{01}Z_{02}}\right]. \tag{5}$$



(a)



(b)

Fig. 9. Output power and phase deviation versus input power of the experimental CCF power amplifier using gate bias control. (a) Gate bias control. (b) Output power and phase deviation versus input power.

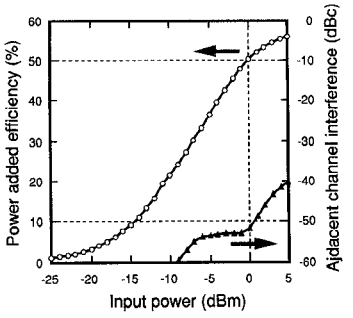


Fig. 10. Power added efficiency and adjacent channel interference in 192 kHz bands at 600 kHz offset frequency from 1.9 GHz versus input power of the experimental CCF power amplifier.

channel interference was measured by using an ANRITSU MG 3670A digital modulation signal generator, an ANRITSU MS8604A digital mobile radio transmitter tester, and a HP 8561E spectrum analyzer.

Since the adjacent channel interference of the Japanese PHS standards are −50 dBc at 600 kHz offset frequency, the measured linearity is well within the specification. The spectra of the output QPSK signal of the CCF PA and the conventional common-source FET PA at 4-dB gain compression is shown in Fig. 11. The adjacent channel interference of the conventional common-source FET PA is −47 dBc. This demonstrates the phase distortion improvement of the CCF PA compared to the CSF PA. The high PAE of 50%, which is higher than the 20–40% PAE reported for other PA's [11], [12], is due to the self phase distortion compensation.

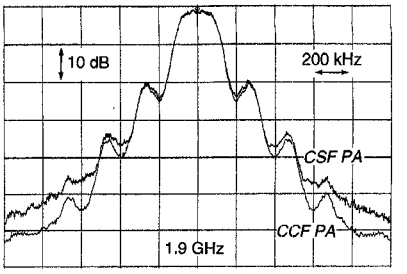


Fig. 11. Output power spectra of CCF PA and CSF PA for 1.9 GHz modulated input.

This enables a small, lightweight PHS handset and long operating time.

This design technique can be applied not only to amplifiers but also to limiters, which need to operate with low phase distortion.

IV. Conclusion

We have presented a self phase distortion compensation technique. The increase in Gd makes the phase deviation increase in the CSF and decrease in the CGF. Since the CCF contains both FET's, the total phase is minimized by the self phase distortion compensation. The validity of the design methods were confirmed. The experimental CCF power amplifier has more than 20-dB gain, 21-dBm output power and 50% PAE at an operating voltage of only 3 V. Among the PA's designed for the PHS handsets, this amplifier achieves the highest efficiency.

Appendix A
Simplified Equivalent Circuit Analysis of CSF

Consider the simplified equivalent CSF circuit model described in Fig. 2(a). It consists of a modified small-signal equivalent circuit. C_{dg}, G_{dg}, and G_{gs}, etc. are ignored to simplify the calculation. This is reasonable since these are considered to be almost constant in the weakly nonlinear region in which the breakdown of the FET does not occur. The relationship between the voltage and current of each node is as follows

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} j\omega C_{gs} & 0 \\ g_m & (j\omega C_{ds} + G_d) \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}. \tag{A1}$$

Then, transforming Y-parameters to S-parameters, S_{21} is given by (A2), as shown at the bottom of the next page, in which Z_{01} and Z_{02} are the input characteristic impedance and output characteristic impedance, respectively. The phase of S_{21} is given by

$$\text{phase}(S_{21}) = \pi - \tan^{-1} \cdot \left[\frac{\omega\{(C_{gs}Z_{01} + C_{ds}Z_{02}) + G_d C_{gs} Z_{01} Z_{02}\}}{1 + G_d Z_{02} - \omega^2 C_{gs} C_{ds} Z_{01} Z_{02}} \right]. \tag{A3}$$

Assuming that

$$f(G_d) = g(C_{gs}) = \frac{\omega\{(C_{gs}Z_{01} + C_{ds}Z_{02}) + G_dC_{gs}Z_{01}Z_{02}\}}{1 + G_dZ_{02} - \omega^2C_{gs}C_{ds}Z_{01}Z_{02}} \quad \text{(A4)}$$

the differentials of the phase of S_{21} are given by

$$\frac{\partial_{\text{phase}}(S_{21})}{\partial G_d} = -\frac{\tan^{-1}\{f(G_d)\}}{\partial f(G_d)} \cdot \frac{\partial f(G_d)}{\partial G_d} = -\frac{1}{1 + \{f(G_d)\}^2}\frac{\partial f(G_d)}{\partial G_d} > 0 \quad \text{(A5)}$$

and

$$\frac{\partial_{\text{phase}}(S_{21})}{\partial C_{gs}} = -\frac{\tan^{-1}\{g(C_{gs})\}}{\partial g(C_{gs})} \cdot \frac{\partial g(C_{gs})}{\partial C_{gs}} = -\frac{1}{1 + \{g(C_{gs})\}^2}\frac{\partial g(C_{gs})}{\partial C_{gs}} < 0. \quad \text{(A6)}$$

II. Appendix B
Simplified Equivalent Circuit Analysis of CGF

Consider the simplified equivalent CGF circuit model described in Fig. 2(b). Furthermore, C_{ds} is ignored to simplify the calculation since this is considered to be almost constant in the weakly nonlinear region. The relationship between the voltage and current of each node is as follows

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} g_m + j\omega C_{gs} + G_d & -G_d \\ -g_m - G_d & G_d \end{bmatrix}\begin{bmatrix} v_1 \\ v_2 \end{bmatrix}. \quad \text{(B1)}$$

Then, transforming Y-parameters to S-parameters, S_{21} is given by

$$S_{21} = \frac{2(g_m + G_d)(Z_{01}Z_{02})^{1/2}}{1 + (g_m + G_d)Z_{01} + G_dZ_{02} + j\omega C_{gs}Z_{01}(1 + G_dZ_{02})} \quad \text{(B2)}$$

in which Z_{01} and Z_{02} are the input characteristic impedance and output characteristic impedance, respectively. The phase of S_{21} is given by

$$\text{phase}(S_{21}) = \tan^{-1}\left[\frac{-\omega C_{gs}Z_{01}(1 + G_dZ_{02})}{1 + (g_m + G_d)Z_{01} + G_dZ_{02}}\right]. \quad \text{(B3)}$$

Assuming that

$$f(G_d) = g(C_{gs}) = \frac{\omega C_{gs}Z_{01}(1 + G_dZ_{02})}{1 + (g_m + G_d)Z_{01} + G_dZ_{02}} \quad \text{(B4)}$$

the differentials are given by

$$\frac{\partial f(G_d)}{\partial G_d} = \frac{-\omega C_{gs}Z_{01}^2(1 - g_mZ_{02})}{\{1 + (g_m + G_d)Z_{01} + G_dZ_{02}\}^2} \quad \text{(B5)}$$

and

$$\frac{\partial g(C_{gs})}{\partial C_{gs}} = \frac{\omega Z_{01}(1 + G_dZ_{02})}{1 + (g_m + G_d)Z_{01} + G_dZ_{02}} > 0. \quad \text{(B6)}$$

Since g_m of the FET for power amplifiers is usually greater than 100 mS, $1 - g_m * Z_{02} < 0$. Thus, the differentials of the phase of S_{21} are given by

$$\frac{\partial_{\text{phase}}(S_{21})}{\partial G_d} = \frac{\tan^{-1}\{-f(G_d)\}}{\partial f(G_d)} \cdot \frac{\partial f(G_d)}{\partial G_d} = -\frac{1}{1 + \{f(G_d)\}^2}\frac{\partial f(G_d)}{\partial G_d} < 0 \quad \text{(B7)}$$

and

$$\frac{\partial_{\text{phase}}(S_{21})}{\partial C_{gs}} = \frac{\tan^{-1}\{-g(C_{gs})\}}{\partial g(C_{gs})} \cdot \frac{\partial g(C_{gs})}{\partial C_{gs}} = -\frac{1}{1 + \{g(C_{gs})\}^2}\frac{\partial g(C_{gs})}{\partial C_{gs}} < 0. \quad \text{(B8)}$$

Appendix C
Simplified Equivalent Circuit Analysis of CCF

Consider the simplified equivalent cascode connection model described in Fig. 7. It combines the CSF with the CGF of Fig. 2. The relationship between the voltage and current of each node is in (C1) as shown at the top of the next page, where g_{m1} and g_{m2} are the transconductances of each FET. Since $C_{gs2} \gg C_{ds1}$, and $g_{m2} \gg G_{d1}, G_{d2}, \omega C_{gs2}$, the approximate expression for this circuit simplifies to

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} j\omega C_{gs1} & 0 \\ g_{m1} & \dfrac{G_{d2}}{g_{m2}}(G_{d1} + j\omega C_{gs2}) \end{bmatrix}\begin{bmatrix} v_1 \\ v_2 \end{bmatrix}. \quad \text{(C2)}$$

Then, transforming Y-parameters to S-parameters, S_{21} is given by (C3) as shown at the top of the next page, in which Z_{01} and Z_{02} are the input characteristic impedance and output characteristic impedance, respectively. The phase of $S_{21}$is given by

$$\text{phase}(S_{21}) = \pi - \tan^{-1} \cdot \left[\frac{\omega\left(C_{gs1}Z_{01} + \dfrac{C_{gs2}G_{d2}}{g_{m2}}Z_{02} + \dfrac{C_{gs1}G_{d1}G_{d2}}{g_{m2}}Z_{01}Z_{02}\right)}{1 + \dfrac{G_{d1}G_{d2}}{g_{m2}}Z_{02} - \omega^2\dfrac{C_{gs1}C_{gs2}G_{d2}}{g_{m2}}Z_{01}Z_{02}}\right]. \quad \text{(C4)}$$

$$S_{21} = \frac{-2g_m(Z_{01}Z_{02})^{1/2}}{\{1 + G_dZ_{02} - \omega^2C_{gs}C_{ds}Z_{01}Z_{02}\} + j\omega\{(C_{gs}Z_{01} + C_{ds}Z_{02}) + G_dC_{gs}Z_{01}Z_{02}\}} \quad \text{(A2)}$$

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} \dfrac{j\omega C_{gs1}}{(g_{m2}+G_{d2})+\{G_{d1}+j\omega(C_{ds1}+C_{gs2})\}} & 0 \\ \dfrac{g_{m1}(g_{m2}+G_{d2})}{(g_{m2}+G_{d2})+\{G_{d1}+j\omega(C_{ds1}+C_{gs2})\}} & \dfrac{G_{d2}\{G_{d1}+j\omega(C_{ds1}+C_{gs2})\}}{(g_{m2}+G_{d2})+\{G_{d1}+j\omega(C_{ds1}+C_{gs2})\}} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}. \tag{C1}$$

$$S_{21} = \frac{-2g_{m1}(Z_{01}Z_{02})^{1/2}}{\left\{1+G_{d1}\dfrac{G_{d2}}{g_{m2}}Z_{02}-\omega^2 C_{gs1}C_{gs2}\dfrac{G_{d2}}{g_{m2}}Z_{01}Z_{02}\right\}+j\omega\left\{C_{gs1}Z_{01}+C_{gs2}\dfrac{G_{d2}}{g_{m2}}Z_{02}+C_{gs1}G_{d1}\dfrac{G_{d2}}{g_{m2}}Z_{01}Z_{02}\right\}} \tag{C3}$$

Assuming that

$$f(G_{d1})=g(C_{gs1})=h(G_{d2})=i(C_{gs2}) = \frac{\omega\left\{\left(C_{gs1}Z_{01}+C_{gs2}\dfrac{G_{d2}}{g_{m2}}Z_{02}\right)+C_{gs1}G_{d1}\dfrac{G_{d2}}{g_{m2}}Z_{01}Z_{02}\right\}}{1+G_{d1}\dfrac{G_{d2}}{g_{m2}}Z_{02}-\omega^2 C_{gs1}C_{gs2}\dfrac{G_{d2}}{g_{m2}}Z_{01}Z_{02}} \tag{C5}$$

the differentials are given by

$$\frac{\partial f(G_{d1})}{\partial G_{d1}} = \frac{-\omega C_{gs2}\dfrac{G_{d2}}{g_{m2}}Z_{02}^2(1+\omega^2 C_{gs1}^2 Z_{01}^2)}{\{1+G_{d1}\dfrac{G_{d2}}{g_{m2}}Z_{02}-\omega^2 C_{gs1}C_{gs2}\dfrac{G_{d2}}{g_{m2}}Z_{01}Z_{02}\}^2} \times \frac{G_{d2}}{g_{m2}}$$

$$\frac{\partial g(C_{gs1})}{\partial C_{gs1}} = \frac{\omega Z_{01}\left\{\omega^2\left(C_{gs2}\dfrac{G_{d2}}{g_{m2}}\right)^2 Z_{02}^2+(1+G_{d1}\dfrac{G_{d2}}{g_{m2}}Z_{02})^2\right\}}{\left\{1+G_{d1}\dfrac{G_{d2}}{g_{m2}}Z_{02}-\omega^2 C_{gs1}C_{gs2}\dfrac{G_{d2}}{g_{m2}}Z_{01}Z_{02}\right\}^2}$$

$$\frac{\partial h(G_{d2})}{\partial G_{d2}} = \frac{\omega C_{gs2}\dfrac{G_{d2}}{g_{m2}}Z_{02}^2(1+\omega^2 C_{gs1}^2 Z_{01}^2)}{\left\{1+G_{d1}\dfrac{G_{d2}}{g_{m2}}Z_{02}-\omega^2 C_{gs1}C_{gs2}\dfrac{G_{d2}}{g_{m2}}Z_{01}Z_{02}\right\}^2} \times \frac{1}{G_{d2}Z_{02}}$$

$$\frac{\partial i(C_{gs2})}{\partial C_{gs2}} = \frac{\omega\dfrac{G_{d2}}{g_{m2}}Z_{02}\left(1+G_{d1}\dfrac{G_{d2}}{g_{m2}}Z_{02}\right)(1+\omega^2 C_{gs1}^2 Z_{01}^2)}{\left\{1+G_{d1}\dfrac{G_{d2}}{g_{m2}}Z_{02}-\omega^2 C_{gs1}C_{gs2}\dfrac{G_{d2}}{g_{m2}}Z_{01}Z_{02}\right\}^2}. \tag{C6}$$

Thus

$$\frac{\partial_{\text{phase}}(S_{21})}{\partial G_{d1}}>0, \quad \frac{\partial_{\text{phase}}(S_{21})}{\partial C_{gs1}}<0, \quad \frac{\partial_{\text{phase}}(S_{21})}{\partial G_{d2}}<0, \quad \frac{\partial_{\text{phase}}(S_{21})}{\partial C_{gs2}}<0. \tag{C7}$$

ACKNOWLEDGMENT

The authors would like to thank Dr. O. Kurita for valuable suggestions and encouragement during this work, and Dr. M. Aikawa for his fruitful discussions.

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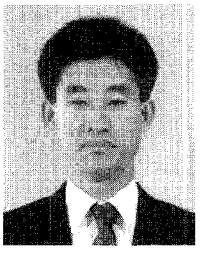
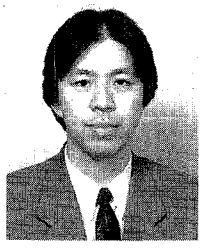


Hitoshi Hayashi (M'94) was born in Nagoya, Japan, on September 20, 1966. He received the B.E. and M.E. degrees in electronics engineering from the University of Tokyo, Tokyo, Japan, in 1990 and 1992, respectively.

In 1992, he joined NTT Radio Communication Systems Laboratories, Yokosuka, Japan, and since then he has been involved in research on GaAs MMIC's. He currently belongs to NTT Wireless Systems Laboratories, Yokosuka, Japan, where he is engaged in the development of microwave amplifiers.

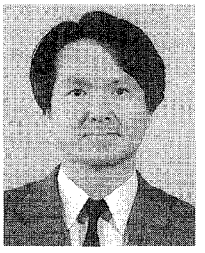
He is a member of the Institute of Electronics, Information and Communication Engineers (IEICE) of Japan.



Masashi Nakatsugawa (M'93) was born in Hamamatsu, Japan, in 1963. He received the B.E. and M.E. degrees in electronics and communication engineering from Waseda University, Tokyo, Japan, in 1987 and 1989, respectively.

In 1989, he joined NTT Radio Communication Systems Laboratories, Yokosuka, Japan, and since then he has been involved in research on GaAs MMIC's. He is currently a Research Engineer of NTT Wireless Systems Laboratories, Yokosuka, Japan, where he is engaged in the development of microwave amplifiers.

Mr. Nakatsugawa is a member of the Institute of Electronics, Information and Communication Engineers (IEICE) of Japan.



Masahiro Muraguchi (S'80–M'83) was born in Kanazawa, Japan, on May 23, 1955. He received the B.S. degree in electrical engineering from the Nagoya Institute of Technology, Japan, in 1978, and the M.S. and Ph.D degrees in physical electronics engineering from the Tokyo Institute of Technology in 1980 and 1983, respectively.

He joined the NTT Atsugi Electrical Communications Laboratories, Nippon Telegraph and Telephone Corporation, in 1983, where he was involved in the design and fabrication of GaAs MMIC's. He is currently engaged in research and development work on MMIC's for personal communications at the NTT Wireless Systems Laboratories, Yokosuka, where he is a Senior Research Engineer and Supervisor.

Dr. Muraguchi was awarded the Ichimura Prize by the New Technology Development Foundation in 1994. He has been on the Editorial Committee of IEICE Transactions on Electronics as an Associate Editor since 1994. He is a member of the Institute of Electronics, Information and Communication Engineers (IEICE) of Japan.